

## VERSION WITH MARKINGS TO SHOW CHANGES MADE

### In the Claims

The claims have been amended as follows:

1           21. (Twice Amended) An optoelectronic semiconductor package device, comprising:  
2           a semiconductor chip that includes an upper surface, a lower surface and four outer side  
3 surfaces between the upper and lower surfaces, wherein the upper surface includes a light  
4 sensitive cell and a conductive pad;  
5           an insulative housing that includes a top surface, a bottom surface and uncurved  
6 peripheral side surfaces between the top and bottom surfaces, wherein the insulative housing  
7 further includes first and second insulative housing portions, the first housing portion is a single-  
8 piece that provides the bottom surface and is non-transparent, and the second housing portion  
9 contacts the upper surface, **is farther from the bottom surface than the lower surface is from**  
10 **the bottom surface**, provides at least a portion of the top surface and is transparent; and  
11           a conductive trace that extends outside the insulative housing and is electrically  
12 connected to the pad inside the insulative housing.

1           31. (Twice Amended) An optoelectronic semiconductor package device, comprising:  
2           a semiconductor chip that includes an upper surface, a lower surface and four outer side  
3 surfaces between the upper and lower surfaces, wherein the upper surface includes a light  
4 sensitive cell and a conductive pad;  
5           an insulative housing that includes a top surface, a bottom surface and peripheral side  
6 surfaces between the top and bottom surfaces, wherein the insulative housing further includes  
7 first and second insulative housing portions, the first housing portion is a single-piece that  
8 provides the bottom surface, the peripheral side surfaces and a peripheral portion of the top  
9 surface, contacts the lower surface and the outer side surfaces, is spaced from the light sensitive  
10 cell and is non-transparent, and the second housing portion is a single-piece or double-piece that  
11 provides a central portion of the top surface within the peripheral portion of the top surface,  
12 contacts the first housing portion, the light sensitive cell and the conductive trace, is spaced from

13 the lower surface, is farther from the bottom surface than the lower surface is from the  
14 bottom surface, is transparent and is exposed; and  
15 a conductive trace that extends outside the insulative housing and is electrically  
16 connected to the pad inside the insulative housing.

1 61. (Amended) An optoelectronic semiconductor package device, comprising:  
2 a semiconductor chip that includes an upper surface, a lower surface and outer side  
3 surfaces between the upper and lower surfaces, wherein the upper surface includes a light  
4 sensitive cell and a conductive pad;  
5 an insulative housing that includes a first single-piece non-transparent insulative housing  
6 portion that **contacts the chip**, covers the lower surface and the side surfaces and is spaced from  
7 the light sensitive cell and a second transparent insulative housing portion that contacts the first  
8 housing portion and the light sensitive cell, is spaced from the lower surface and is exposed; and  
9 a conductive trace that extends through an opening in the first housing portion, extends  
10 outside the insulative housing and is electrically connected to the pad inside the insulative  
11 housing.

1 66. (Amended) An optoelectronic semiconductor package device, comprising:  
2 a semiconductor chip that includes an upper surface, a lower surface and outer side  
3 surfaces between the upper and lower surfaces, wherein the upper surface includes a light  
4 sensitive cell and a conductive pad;  
5 an insulative housing that includes a first single-piece non-transparent insulative housing  
6 portion that **contacts the chip**, covers the lower surface and the side surfaces and is spaced from  
7 the light sensitive cell and a second transparent insulative housing portion that contacts the first  
8 housing portion and the light sensitive cell, is spaced from the lower surface and is exposed; and  
9 a conductive trace that extends through an opening in the first housing portion, extends  
10 outside the insulative housing, is bent outside the insulative housing and is electrically connected  
11 to the pad inside the insulative housing.

1           71. (Amended) An optoelectronic semiconductor package device, comprising:  
2           a semiconductor chip that includes an upper surface, a lower surface and outer side  
3 surfaces between the upper and lower surfaces, wherein the upper surface includes a light  
4 sensitive cell and a conductive pad;  
5           an insulative housing that includes a first single-piece non-transparent insulative housing  
6 portion that **contacts the chip**, covers the lower surface and the side surfaces and is spaced from  
7 the light sensitive cell and a second transparent insulative housing portion that contacts the first  
8 housing portion and the light sensitive cell, is spaced from the lower surface and is exposed; and  
9           a conductive trace that extends through an opening in the first housing portion, extends  
10 outside the insulative housing, does not contact an insulative material outside the first housing  
11 portion and is electrically connected to the pad inside the insulative housing.

1           76. (Amended) An optoelectronic semiconductor package device, comprising:  
2           a semiconductor chip that includes an upper surface, a lower surface and outer side  
3 surfaces between the upper and lower surfaces, wherein the upper surface includes a light  
4 sensitive cell and a conductive pad;  
5           an insulative housing that includes a first single-piece non-transparent insulative housing  
6 portion that covers the lower surface and the side surfaces and is spaced from the light sensitive  
7 cell and a second transparent insulative housing portion that contacts the first housing portion  
8 and the light sensitive cell, is spaced from the lower surface and is exposed; and  
9           a conductive trace that **includes a lead and a planar metal trace, wherein the lead**  
10 extends through an opening in the first housing portion, extends outside the insulative housing  
11 and is electrically connected to the pad inside the insulative housing, **and the planar** ~~wherein the~~  
12 ~~conductive trace includes a plated-metal trace~~ **contacts and is not integral with the lead, that**  
13 extends across one of the side surfaces and does not extend outside the insulative housing.

1           81. (Amended) An optoelectronic semiconductor package device, comprising:  
2           a semiconductor chip that includes an upper surface, a lower surface and outer side  
3 surfaces between the upper and lower surfaces, wherein the upper surface includes a light  
4 sensitive cell and a conductive pad;

5 an insulative housing that includes a first single-piece non-transparent insulative housing  
6 portion that covers the lower surface and the side surfaces and is spaced from the light sensitive  
7 cell and a second transparent insulative housing portion that contacts the first housing portion  
8 and the light sensitive cell, is spaced from the lower surface and is exposed; and

9 a conductive trace that **includes a lead and a planar metal trace, wherein the lead**  
10 extends through an opening in the first housing portion, extends outside the insulative housing  
11 and is electrically connected to the pad inside the insulative housing, **and the planar** ~~wherein the~~  
12 ~~conductive trace includes a plated-metal trace that~~ **contacts and is not integral with the lead,**  
13 contacts the first and second housing portions, extends across one of the side surfaces and does  
14 not extend outside the insulative housing.

1 86. (Amended) An optoelectronic semiconductor package device, comprising:  
2 a semiconductor chip that includes an upper surface, a lower surface and outer side  
3 surfaces between the upper and lower surfaces, wherein the upper surface includes a light  
4 sensitive cell and a conductive pad;

5 an insulative housing that includes a first single-piece non-transparent insulative housing  
6 portion that covers the lower surface and the side surfaces and is spaced from the light sensitive  
7 cell and a second transparent insulative housing portion that contacts the first housing portion  
8 and the light sensitive cell, is spaced from the lower surface and is exposed; and

9 a conductive trace that **includes a lead and a planar metal trace, wherein the lead**  
10 extends through an opening in the first housing portion, extends outside the insulative housing  
11 and is electrically connected to the pad inside the insulative housing, **and the planar** ~~wherein the~~  
12 ~~conductive trace includes a plated-metal trace that~~ **contacts and is not integral with the lead,**  
13 contacts the first and second housing portions, overlaps the pad, extends across one of the side  
14 surfaces and does not extend outside the insulative housing.

1 91. (Amended) An optoelectronic semiconductor package device, comprising:  
2 a semiconductor chip that includes an upper surface, a lower surface and four outer side  
3 surfaces between the upper and lower surfaces, wherein the upper surface includes a light  
4 sensitive cell and a conductive pad;

an insulative housing that includes a top surface, a bottom surface and peripheral side surfaces between the top and bottom surfaces, wherein the insulative housing further includes first and second insulative housing portions, the first housing portion is a single-piece that **contacts the chip**, covers the lower surface and the outer side surfaces and provides the bottom surface, the peripheral side surfaces and a peripheral portion of the top surface and is non-transparent, the second housing portion contacts the first housing portion and the light sensitive cell, provides a central portion of the top surface within the peripheral portion of the top surface and is transparent, and the top surface is exposed; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

96. (Amended) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a top surface, a bottom surface and peripheral side surfaces between the top and bottom surfaces, wherein the insulative housing further includes first and second insulative housing portions, the first housing portion is a single-piece that **contacts the chip**, covers the lower surface and the outer side surfaces and provides the bottom surface, the peripheral side surfaces and a peripheral portion of the top surface and is non-transparent, the second housing portion contacts the first housing portion and the light sensitive cell, provides a central portion of the top surface within the peripheral portion of the top surface and is transparent, the first housing portion is exposed at the top surface, bottom surface and peripheral side surfaces, and the second housing portion is exposed at the top surface; and

a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

1           101. (Amended) An optoelectronic semiconductor package device, comprising:  
2           a semiconductor chip that includes an upper surface, a lower surface and four outer side  
3 surfaces between the upper and lower surfaces, wherein the upper surface includes a light  
4 sensitive cell and a conductive pad;  
5           an insulative housing that includes a top surface, a bottom surface and peripheral side  
6 surfaces between the top and bottom surfaces, wherein the insulative housing further includes  
7 first and second insulative housing portions, the first housing portion is a single-piece that  
8 **contacts the chip**, covers the lower surface and the outer side surfaces and provides the bottom  
9 surface, the peripheral side surfaces and a peripheral portion of the top surface and is non-  
10 transparent, the second housing portion contacts the first housing portion and the light sensitive  
11 cell, provides a central portion of the top surface within the peripheral portion of the top surface  
12 and is transparent, the central portion of the top surface is recessed relative to the peripheral  
13 portion of the top surface, and the top surface is exposed; and  
14           a conductive trace that extends outside the insulative housing and is electrically  
15 connected to the pad inside the insulative housing.

1           106. (Amended) An optoelectronic semiconductor package device, comprising:  
2           a semiconductor chip that includes an upper surface, a lower surface and four outer side  
3 surfaces between the upper and lower surfaces, wherein the upper surface includes a light  
4 sensitive cell and a conductive pad;  
5           an insulative housing that includes a top surface, a bottom surface and peripheral side  
6 surfaces between the top and bottom surfaces, wherein the insulative housing further includes  
7 first and second insulative housing portions, the first housing portion is a single-piece that  
8 **contacts the chip**, covers the lower surface and the outer side surfaces and provides the bottom  
9 surface, the peripheral side surfaces and a peripheral portion of the top surface and is non-  
10 transparent, the second housing portion contacts the first housing portion and the light sensitive  
11 cell, provides a central portion of the top surface within the peripheral portion of the top surface  
12 and is transparent, the central portion of the top surface is recessed relative to the peripheral  
13 portion of the top surface, the first housing portion is exposed at the top surface, bottom surface  
14 and peripheral side surfaces, and the second housing portion is exposed at the top surface; and

15 a conductive trace that extends outside the insulative housing and is electrically  
16 connected to the pad inside the insulative housing.

1 111. (Amended) An optoelectronic semiconductor package device, comprising:  
2 a semiconductor chip that includes an upper surface, a lower surface and four outer side  
3 surfaces between the upper and lower surfaces, wherein the upper surface includes a light  
4 sensitive cell and a conductive pad;  
5 an insulative housing that includes a top surface, a bottom surface and peripheral side  
6 surfaces between the top and bottom surfaces, wherein the insulative housing further includes  
7 first and second insulative housing portions, the first housing portion is a single-piece that  
8 **contacts the chip**, covers the lower surface and the outer side surfaces and provides the bottom  
9 surface, the peripheral side surfaces and a peripheral portion of the top surface and is non-  
10 transparent, the second housing portion contacts the first housing portion and the light sensitive  
11 cell, provides a central portion of the top surface within the peripheral portion of the top surface  
12 and is transparent, and the top, bottom and peripheral side surfaces are exposed; and  
13 a conductive trace that extends outside the insulative housing, is located between the  
14 second housing portion and the chip inside the insulative housing, is spaced from the top surface  
15 and is electrically connected to the pad inside the insulative housing.

1 116. (Amended) An optoelectronic semiconductor package device, comprising:  
2 a semiconductor chip that includes an upper surface, a lower surface and four outer side  
3 surfaces between the upper and lower surfaces, wherein the upper surface includes a light  
4 sensitive cell and a conductive pad;  
5 an insulative housing that includes a top surface, a bottom surface and peripheral side  
6 surfaces between the top and bottom surfaces, wherein the insulative housing further includes  
7 first and second insulative housing portions, the first housing portion is a single-piece that  
8 **contacts the chip**, covers the lower surface and the outer side surfaces and provides the bottom  
9 surface, the peripheral side surfaces and a peripheral portion of the top surface and is non-  
10 transparent, the second housing portion contacts the first housing portion and the light sensitive

11 cell, provides a central portion of the top surface within the peripheral portion of the top surface  
12 and is transparent, and the top, bottom and peripheral side surfaces are exposed; and  
13 a conductive trace that extends outside the insulative housing, includes a top surface that  
14 faces away from the chip and contacts the second housing portion inside the insulative housing,  
15 includes a bottom surface that faces towards the chip and contacts the second housing portion  
16 inside the insulative housing, is spaced from the top and bottom surfaces, extends through one of  
17 the peripheral side surfaces and is electrically connected to the pad inside the insulative housing.

1 121. (Amended) An optoelectronic semiconductor package device, comprising:  
2 a semiconductor chip that includes an upper surface, a lower surface and four outer side  
3 surfaces between the upper and lower surfaces, wherein the upper surface includes a light  
4 sensitive cell and a conductive pad;  
5 an insulative housing that includes first and second insulative housing portions, wherein  
6 the first housing portion is a single-piece that covers the lower surface and the outer side surfaces  
7 and includes a top surface, a bottom surface, peripheral side surfaces between the top and bottom  
8 surfaces, a peripheral ledge at the top surface, and inner side surfaces inside the peripheral ledge  
9 opposite the peripheral side surfaces that extend from the top surface towards the bottom surface  
10 and are spaced from the bottom surface and is non-transparent, and the second housing portion is  
11 located within and recessed relative to the peripheral ledge, contacts the light sensitive cell, **does**  
12 **not extend midway between the upper and lower surfaces outside the chip** and is  
13 transparent; and  
14 a conductive trace that extends outside the insulative housing and is electrically  
15 connected to the pad inside the insulative housing.

1 126. (Amended) An optoelectronic semiconductor package device, comprising:  
2 a semiconductor chip that includes an upper surface, a lower surface and four outer side  
3 surfaces between the upper and lower surfaces, wherein the upper surface includes a light  
4 sensitive cell and a conductive pad;  
5 an insulative housing that includes first and second insulative housing portions, wherein  
6 the first housing portion is a single-piece that includes a top surface, a bottom surface, peripheral



7 side surfaces between the top and bottom surfaces, a peripheral ledge at the top surface, and inner  
8 side surfaces inside the peripheral ledge opposite the peripheral side surfaces that extend from  
9 the top surface towards the bottom surface and are spaced from the bottom surface and is non-  
10 transparent, the second housing portion is located within and recessed relative to the peripheral  
11 ledge, contacts the light sensitive cell, **does not extend midway between the upper and lower**  
12 **surfaces outside the chip** and is transparent, the first housing portion is exposed at the top  
13 surface, bottom surface and peripheral side surfaces, and the second housing portion is exposed  
14 at the top surface; and  
15 a conductive trace that extends outside the insulative housing and is electrically  
16 connected to the pad inside the insulative housing.

1 131. (Amended) An optoelectronic semiconductor package device, comprising:  
2 a semiconductor chip that includes an upper surface, a lower surface and four outer side  
3 surfaces between the upper and lower surfaces, wherein the upper surface includes a light  
4 sensitive cell and a conductive pad;  
5 an insulative housing that includes first and second insulative housing portions, wherein  
6 the first housing portion is a single-piece that covers the lower surface and the outer side surfaces  
7 and includes a top surface, a bottom surface, peripheral side surfaces between the top and bottom  
8 surfaces, a peripheral ledge at the top surface, and inner side surfaces inside the peripheral ledge  
9 opposite the peripheral side surfaces that extend from the top surface towards the bottom surface  
10 and are spaced from the bottom surface and is non-transparent, and the second housing portion is  
11 located within and recessed relative to the peripheral ledge, contacts the light sensitive cell and  
12 the inner side surfaces, **does not extend midway between the upper and lower surfaces**  
13 **outside the chip** and is transparent; and  
14 a conductive trace that extends outside the insulative housing and is electrically  
15 connected to the pad inside the insulative housing.

1           136. (Amended) An optoelectronic semiconductor package device, comprising:  
2           a semiconductor chip that includes an upper surface, a lower surface and four outer side  
3 surfaces between the upper and lower surfaces, wherein the upper surface includes a light  
4 sensitive cell and a conductive pad;  
5           an insulative housing that includes first and second insulative housing portions, wherein  
6 the first housing portion is a single-piece that covers the lower surface and the outer side surfaces  
7 and includes a top surface, a bottom surface, peripheral side surfaces between the top and bottom  
8 surfaces, a peripheral ledge at the top surface, and inner side surfaces inside the peripheral ledge  
9 opposite the peripheral side surfaces that extend from the top surface towards the bottom surface  
10 and are spaced from the bottom surface and is non-transparent, the second housing portion is  
11 located within and recessed relative to the peripheral ledge, contacts the light sensitive cell and  
12 the inner side surfaces, **does not extend midway between the upper and lower surfaces**  
13 **outside the chip** and is transparent, the first housing portion is exposed at the top surface,  
14 bottom surface and peripheral side surfaces, and the second housing portion is exposed at the top  
15 surface; and  
16           a conductive trace that extends outside the insulative housing and is electrically  
17 connected to the pad inside the insulative housing.

1           141. (Amended) An optoelectronic semiconductor package device, comprising:  
2           a semiconductor chip that includes an upper surface, a lower surface and four outer side  
3 surfaces between the upper and lower surfaces, wherein the upper surface includes a light  
4 sensitive cell and a conductive pad;  
5           an insulative housing that includes first and second insulative housing portions, wherein  
6 the first housing portion is a single-piece that covers the lower surface and the outer side surfaces  
7 and includes a top surface, a bottom surface, uncurved peripheral side surfaces between the top  
8 and bottom surfaces, a peripheral ledge at the top surface, and ~~uncurved~~ inner side surfaces inside  
9 the peripheral ledge opposite the peripheral side surfaces that extend from the top surface  
10 towards the bottom surface and are spaced from the bottom surface and is non-transparent, and  
11 the second housing portion **extends into** ~~is located within and recessed relative to~~ the peripheral

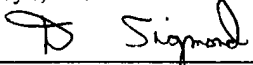
12 ledge, contacts the light sensitive cell, **does not extend midway between the upper and lower**  
13 **surfaces outside the chip** and is transparent; and  
14 a conductive trace that extends outside the insulative housing and is electrically  
15 connected to the pad inside the insulative housing.

1 146. (Amended) An optoelectronic semiconductor package device, comprising:  
2 a semiconductor chip that includes an upper surface, a lower surface and four outer side  
3 surfaces between the upper and lower surfaces, wherein the upper surface includes a light  
4 sensitive cell and a conductive pad;  
5 an insulative housing that includes first and second insulative housing portions, wherein  
6 the first housing portion is a single-piece that covers the lower surface and the outer side surfaces  
7 and includes a top surface, a bottom surface, uncurved peripheral side surfaces between the top  
8 and bottom surfaces, a peripheral ledge at the top surface, and ~~uncurved~~ inner side surfaces inside  
9 the peripheral ledge opposite the peripheral side surfaces that extend from the top surface  
10 towards the bottom surface and are spaced from the bottom surface and is non-transparent, the  
11 second housing portion **extends into** ~~is located within and recessed relative to~~ the peripheral  
12 ledge, contacts the light sensitive cell, **does not extend midway between the upper and lower**  
13 **surfaces outside the chip** and is transparent, the first housing portion is exposed at the top  
14 surface, bottom surface and peripheral side surfaces, and the second housing portion is exposed  
15 at the top surface; and  
16 a conductive trace that extends outside the insulative housing and is electrically  
17 connected to the pad inside the insulative housing.

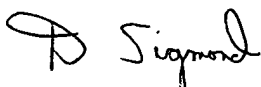
## REMARKS

Claim 1-150 are pending. In this Supplemental Response, claims 31, 41, 61, 66, 71, 76, 81, 86, 91, 96, 101, 106, 111, 116, 121, 126, 131, 136, 141 and 146 have been amended. No new matter has been added.

The application is believed to be in condition for allowance. Should any issues remain, the Examiner is encouraged to telephone the undersigned attorney.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on May 1, 2003.	
	<u>5, 1, 03</u>
David M. Sigmond Attorney for Applicant	Date of Signature

Respectfully submitted,



David M. Sigmond  
Attorney for Applicant  
Reg. No. 34,013  
(303) 554-8371  
(303) 554-8667 (fax)